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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EL

Office Action Summary	Application No.	Applicant(s)	
	10/649,311	BASCERI ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) *5-7,10,21-23,36,42,43,45,48 and 51-53* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 8-17, 24-34, 44, 46, 47, 49-50, 54-60* is/are rejected.

7)☒ Claim(s) *2, 4, 18, 19, 20, 35, 37, 38, 39, 40, 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

In view of Applicant's amendment to the claim, the objection to claim 3 is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 8-9, 11-17, 24-33, 50, and 54-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (U.S. Patent No. 6,458,653) in view of Won et al. (U.S. Patent No. 6,667,209).

In re claim 1, Jang et al. disclose the method of forming a capacitor sequentially comprising:

forming an inwardly-tapered-sidewall spacer (116, see column 3, line 60 through column 4, line 51) within an opening of a capacitor electrode-forming layer (110);

anisotropically etching the spacer (see column 4, line 64 through column 5, line 3);

after anisotropically etching the spacer, depositing a first capacitor electrode layer (121) over the inwardly-tapered-sidewall spacer within the opening.

Jang et al. disclose the method of forming a lower electrode for a DRAM (see column 5, lines 22-37), but do not explicitly disclose the method of forming the capacitor

dielectric and the second capacitor electrode layer. While it is known to complete the fabrication of a DRAM capacitor, a capacitor dielectric and a second capacitor electrode must be formed, the examiner has provided a reference that discloses these steps.

Won et al. disclose the method of forming a capacitor dielectric region (200) and then a second capacitor electrode layer (210) over the first capacitor electrode layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dielectric layer and a second capacitor electrode in the method of Jang et al. in order to complete the fabrication of the DRAM and create and operable device.

In re claim 8, Jang et al. disclose the method wherein the opening comprises sidewalls and the inwardly-tapered-sidewall spacer resides over at least upper portions of the sidewalls (see Figure 6).

In re claim 9, Jang et al. disclose the method wherein the opening comprises sidewalls and the inwardly-tapered-sidewall spacer resides over an entirety of the sidewalls (see Figure 6).

In re claim 11, Jang et al. discloses the method wherein the opening comprises sidewalls and the capacitor electrode-forming layer comprises an elevationally outermost surface proximate the opening, the sidewalls including straight linear portions which are angled from normal to the elevationally outermost surface (see Figure 6).

In re claims 12, 13, and 14, Jang et al. disclose the method wherein the straight linear portions are angled from normal to the elevationally outermost surface (see Figure 6 and column 3, line 60 through column 4, line 32) and disclose a Figure in which the angle is at least 5 degrees or at least 10 degrees. Jang et al. do not explicitly

disclose the angle of the sidewall, and therefore, do not disclose the method wherein the angle of the sidewall is at least 15 degrees from normal to the elevationally outermost surface. The examiner notes that Applicant does not teach that the angle of the sidewall solves any stated problem or is for any particular purpose. Therefore, the sidewall angle lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the sidewall angle at 15 degrees rather than the disclosed 10 degrees since the invention would perform equally well when the sidewall is formed at different angles with respect to normal and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 15, Jang et al disclose the method wherein the sidewall spacer comprises laterally inner sidewall portions, the laterally inner sidewall portions including straight linear portions which are angled normal to the elevationally outermost surface (see Figure 6).

In re claim 16, Jang et al. disclose the method further comprising removing at least a portion of the inwardly-tapered-sidewall spacer after the depositing and prior to forming the capacitor dielectric region (see column 4, lines 64-67 or column 5, lines 15-37, column 6, lines 63-65, and Figures 12-13).

In re claim 17, Jang et al. discloses the method of forming a capacitor comprising:

providing a substrate (100) having a capacitor electrode-forming layer (110) thereon, the capacitor electrode-forming layer having an opening;

forming a sidewall spacer (116) within the opening, the sidewall spacer being laterally thicker at an elevationally outer portion within the opening as compared to an elevationally inner portion within the opening (see Figure 6, 116, see column 3, line 60 through column 4, line 51);

anisotropically etching the spacer (see column 4, line 64 through column 5, line 3);

after anisotropically etching the spacer, forming a first capacitor electrode layer (121) within the opening laterally over the sidewall spacer;

and removing at least a portion of the sidewall spacer (see column 4, lines 64-67 or column 5, lines 15-37, column 6, lines 63-65, and Figures 12-13).

Jang et al. disclose the method of forming a lower electrode for a DRAM (see column 5, lines 22-37), but do not explicitly disclose the method of forming the capacitor dielectric and the second capacitor electrode layer. While it is known to complete the fabrication of a DRAM capacitor, a capacitor dielectric and a second capacitor electrode must be formed, the examiner has provided a reference that discloses these steps.

Won et al. disclose the method of forming a capacitor dielectric region (200) and then a second capacitor electrode layer (210) over the first capacitor electrode layer. It would have been obvious to one of ordinary skill in the art at the time the invention was

made to form a dielectric layer and a second capacitor electrode in the method of Jang et al. in order to complete the fabrication of the DRAM and create and operable device.

In re claim 24, Jang et al. disclose the method wherein the opening comprises sidewalls and the inwardly-tapered-sidewall spacer resides over at least upper portions of the sidewalls (see Figure 6).

In re claim 25, Jang et al. disclose the method wherein the opening comprises sidewalls and the inwardly-tapered-sidewall spacer resides over an entirety of the sidewalls (see Figure 6).

In re claim 26, Jang et al. discloses the method wherein the opening comprises sidewalls and the capacitor electrode-forming layer comprises an elevationally outermost surface proximate the opening, the sidewalls including straight linear portions which are angled from normal to the elevationally outermost surface (see Figure 6).

In re claims 27, 28, and 29, Jang et al. disclose the method wherein the the straight linear portions are angled from normal to the elevationally outermost surface (see Figure 6 and column 3, line 60 through column 4, line 32) and disclose a Figure in which the angle is at least 5 degrees or at least 10 degrees. Jang et al. do not explicitly disclose the angle of the sidewall, and therefore, do not disclose the method wherein the angle of the sidewall is at least 15 degrees from normal to the elevationally outermost surface. The examiner notes that Applicant does not teach that the angle of the sidewall solves any stated problem or is for any particular purpose. Therefore, the sidewall angle lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in

the art at the time the invention was made to form the sidewall angle at 15 degrees rather than the disclosed 10 degrees since the invention would perform equally well when the sidewall is formed at different angles with respect to normal and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 30, Jang et al disclose the method wherein the sidewall spacer comprises laterally inner sidewall portions, the laterally inner sidewall portions including straight linear portions which are angled normal to the elevationally outermost surface (see Figure 6).

In re claims 31 and 32, Jang et al. disclose the method further comprising removing at least a majority or substantially all of the sidewall spacer (column 5, lines 15-37, column 6, lines 63-65, and Figures 12-13).

In re claim 33, Jang et al. discloses the method of forming a capacitor comprising:

forming an opening within a capacitor electrode-forming layer (110) over a substrate, the opening comprising sidewalls;

depositing a spacing layer (116) over the capacitor electrode-forming layer to within the opening over at least upper portions of the sidewalls, the depositing forming the spacing layer to be laterally thicker at an elevationally outer portion within the

opening as compared to an elevationally inner portion within the opening (see Figure 6, 116, see column 3, line 60 through column 4, line 51);

anisotropically etching the spacing layer to form a spacer within the opening, the spacer being laterally thicker at an elevationally outer portion within the opening as compared to an elevationally inner portion within the opening (see column 4, line 64 through column 5, line 3);

forming a first capacitor electrode layer (121) within the opening laterally over the spacer; and

after forming the first capacitor electrode layer, removing at least a portion of the spacer (see column 4, lines 64-67 or column 5, lines 15-37, column 6, lines 63-65, and Figures 12-13).

Jang et al. disclose the method of forming a lower electrode for a DRAM (see column 5, lines 22-37), but do not explicitly disclose the method of forming the capacitor dielectric and the second capacitor electrode layer. While it is known to complete the fabrication of a DRAM capacitor, a capacitor dielectric and a second capacitor electrode must be formed, the examiner has provided a reference that discloses these steps.

Won et al. disclose the method of forming a capacitor dielectric region (200) and then a second capacitor electrode layer (210) over the first capacitor electrode layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dielectric layer and a second capacitor electrode in the method of Jang et al. in order to complete the fabrication of the DRAM and create and operable device.

In re claim 50, Jang et al. disclose the method wherein the opening comprises sidewalls and the inwardly-tapered-sidewall spacer resides over an entirety of the sidewalls (see Figure 6).

In re claim 54, Jang et al. discloses the method wherein the opening comprises sidewalls and the capacitor electrode-forming layer comprises an elevationally outermost surface proximate the opening, the sidewalls including straight linear portions which are angled from normal to the elevationally outermost surface (see Figure 6).

In re claims 55, 56, and 57, Jang et al. disclose the method wherein the the straight linear portions are angled from normal to the elevationally outermost surface (see Figure 6 and column 3, line 60 through column 4, line 32) and disclose a Figure in which the angle is at least 5 degrees or at least 10 degrees. Jang et al. do not explicitly disclose the angle of the sidewall, and therefore, do not disclose the method wherein the angle of the sidewall is at least 15 degrees from normal to the elevationally outermost surface. The examiner notes that Applicant does not teach that the angle of the sidewall solves any stated problem or is for any particular purpose. Therefore, the sidewall angle lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the sidewall angle at 15 degrees rather than the disclosed 10 degrees since the invention would perform equally well when the sidewall is formed at different angles with respect to normal and because it has been held that where the general conditions of a claim are disclosed in the prior art,

discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 58, Jang et al disclose the method wherein the sidewall spacer comprises laterally inner sidewall portions, the laterally inner sidewall portions including straight linear portions which are angled normal to the elevationally outermost surface (see Figure 6).

In re claims 59 and 60, Jang et al. disclose the method further comprising removing at least a majority or substantially all of the sidewall spacer (column 5, lines 15-37, column 6, lines 63-65, and Figures 12-13).

Claims 3 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (U.S. Patent No. 6,458,653) and Won et al. (U.S. Patent No. 6,667,209) in view of Deboer et al (U.S. Patent Appl. 2002/0064934).

Jang et al. and Won et al. disclose the method as claimed and rejected above, including the method of forming the capacitor electrode-forming layer of a TEOS oxide, but do not disclose the method wherein the capacitor electrode-forming layer comprises borophosphosilicate glass (BPSG). Deboer et al. disclose the method of utilizing either BPSG and TEOS as an interlayer dielectric layer (see [0036] and [0038]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the interlayer dielectric of the combined Jang et al. and Won et al. with BPSG because as Deboer et al. teaches, BPSG and TEOS oxide are interchangeable in the art for interlayer dielectrics and since it has been held that the selection of a known

material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Claims 44, 46, 47, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (U.S. Patent No. 6,458,653), Won et al. (U.S. Patent No. 6,667,209), and Deboer et al (U.S. Patent Appl. 2002/0064934) in view of Yieh et al. (U.S. Patent No. 6,599,574).

The combined Jang et al. Won et al. and Deboer et al disclose the method as claimed and rejected above, but do not disclose the method of forming the spacing layer with a pressure greater than 10 Torr or 20 Torr and temperature above 600 or 700 degrees Celsius. Yieh et al. disclose the method of forming a BPSG layer at a pressure greater than 10 Torr or 20 Torr and a temperature above 600 or 700 degrees Celsius (see column 14, lines 30-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the BPSG layer at these conditions, because as Yieh et al. teach, the method allows for formation of a BPSG layer with improved film uniformity, higher deposition rate, superior gap fill/reflow capability and smoother surface morphology (see abstract).

Response to Arguments

Applicant's arguments filed September 6, 2005 with respect to the Jang et al. reference have been fully considered but they are not persuasive. Applicant argues that neither Jang et al. nor Oh et al. disclose an anisotropic etching process. The examiner

disagrees and notes that the etching that as disclosed in Jang et al. in column 4, line 64 through column 5, line 3 and Figure 6, 8, 10 disclose anisotropic etching. When etching proceeds in all directions it is defined as isotropic. By definition, any etching that is not isotropic is anisotropic (see Wolf et al. (Silicon Processing for the VLSI Era, Volume 1-Process Technology, Second Edition pages 657-658). As seen in Figure 10 of Jang et al. the etching of the spacer 116 is directional, and more specifically vertical, and thus anisotropic by definition.

Applicant's arguments, see page 16 of the response, filed September 6, 2005, with respect to the Oh et al. in combination with the claim amendments have been fully considered and are persuasive. The 103 rejection of claims 1, 2, 17, 18, 33, and 35 with Oh (U.S. Patent Appl. 2003/0001268) in view of Jang et al. (U.S. Patent No. 6,458,653) has been withdrawn. Further, the 103 rejections of claims 4, 20, and 37 with Oh (U.S. Patent Appl. 2003/0001268) and Jang et al. (U.S. Patent No. 6,458,653) in view of Wofford et al. (U.S. Patent No. 6,686,237) and claims 19, and 38-41 with Oh (U.S. Patent Appl. 2003/0001268) and Jang et al. (U.S. Patent No. 6,458,653) in view of Wang et al. (U.S. Patent No. 6,214,714) are withdrawn.

Allowable Subject Matter

Claims 2, 4, 18-20, 35, and 37-41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Further, claims dependent on the allowed claims would be subject to rejoinder.

The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination, fails to anticipate or render obvious, the method including the limitations of forming an inwardly-tapered sidewall spacer of titanium nitride within an opening of a capacitor electrode-forming layer, anisotropically etching the spacer and after etching the spacer, depositing a first capacitor electrode layer over the inwardly-tapered sidewall spacer within the opening in combination with the other limitations of the claims.

The examiner notes in one embodiment of Oh et al. the method of etching the spacer prior to forming the bottom electrode is discloses, however in that embodiment the material of the spacer is silicon nitride. Further, Oh et al. teach the method of utilizing a titanium nitride spacer, but do not disclose the method wherein the spacer is etched prior to depositing the bottom electrode. Further, Oh et al. does not teach the method of anisotropically etching a TiN spacer. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk